



Schottky Bipolar 8224

CLOCK GENERATOR AND DRIVER FOR 8080A CPU

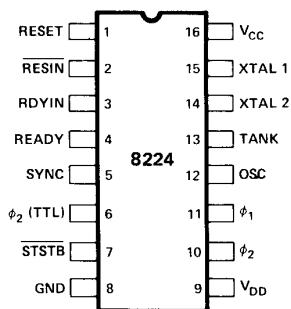
- Single Chip Clock Generator/Driver for 8080A CPU
- Power-Up Reset for CPU
- Ready Synchronizing Flip-Flop
- Advanced Status Strobe
- Oscillator Output for External System Timing
- Crystal Controlled for Stable System Operation
- Reduces System Package Count

The 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer, to meet a variety of system speed requirements.

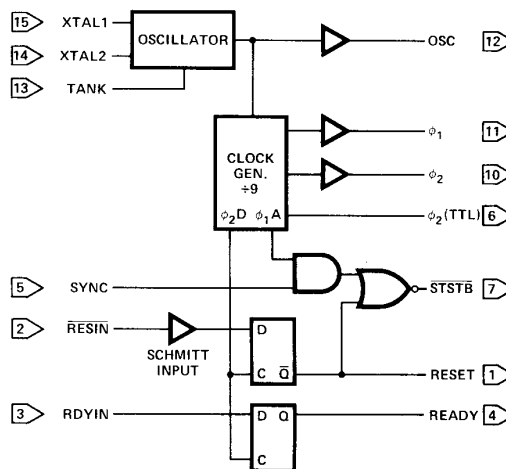
Also included are circuits to provide power-up reset, advance status strobe and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
phi_1	8080
phi_2	CLOCKS

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
phi_2 (TTL)	phi_2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

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FUNCTIONAL DESCRIPTION

General

The 8224 is a single chip Clock Generator/Driver for the 8080A CPU. It contains a crystal-controlled oscillator, a "divide by nine" counter, two high-level drivers and several auxiliary logic functions.

Oscillator

The oscillator circuit derives its basic operating frequency from an external, series resonant, fundamental mode crystal. Two inputs are provided for the crystal connections (XTAL1, XTAL2).

The selection of the external crystal frequency depends mainly on the speed at which the 8080A is to be run at. Basically, the oscillator operates at 9 times the desired processor speed.

A simple formula to guide the crystal selection is:

$$\text{Crystal Frequency} = \frac{1}{t_{CY}} \text{ times } 9$$

Example 1: (500ns t_{CY})
2mHz times 9 = 18mHz*

Example 2: (800ns t_{CY})
1.25mHz times 9 = 11.25mHz

Another input to the oscillator is TANK. This input allows the use overtone mode crystals. This type of crystal generally has much lower "gain" than the fundamental type so an external LC network is necessary to provide the additional "gain" for proper oscillator operation. The external LC network is connected to the TANK input and is AC coupled to ground. See Figure 4.

The formula for the LC network is:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

The output of the oscillator is buffered and brought out on OSC (pin 12) so that other system timing signals can be derived from this stable, crystal-controlled source.

*When using crystals above 10mHz a small amount of frequency "trimming" may be necessary to produce the exact desired frequency. The addition of a small selected capacitance (3pF - 10pF) in series with the crystal will accomplish this function.

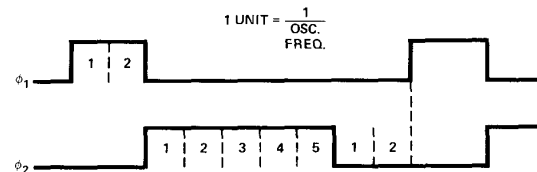
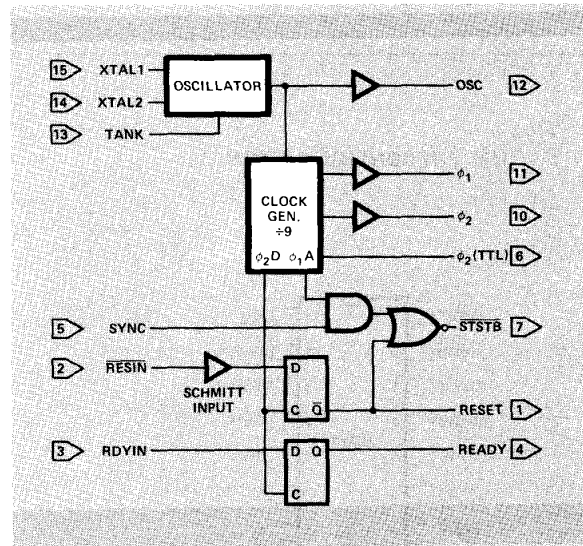
Clock Generator

The Clock Generator consists of a synchronous "divide by nine" counter and the associated decode gating to create the waveforms of the two 8080A clocks and auxiliary timing signals.

The waveforms generated by the decode gating follow a simple 2-5-2 digital pattern. See Figure 2. The clocks generated; phase 1 and phase 2, can best be thought of as consisting of "units" based on the oscillator frequency. Assume that one "unit" equals the period of the oscillator frequency. By multiplying the number of "units" that are contained in a pulse width or delay, times the period of the oscillator frequency, the approximate time in nanoseconds can be derived.

The outputs of the clock generator are connected to two high level drivers for direct interface to the 8080A CPU. A TTL level phase 2 is also brought out ϕ_2 (TTL) for external timing purposes. It is especially useful in DMA dependant activities. This signal is used to gate the requesting device on to the bus once the 8080A CPU issues the Hold Acknowledgement (HLDA).

Several other signals are also generated internally so that optimum timing of the auxiliary flip-flops and status strobe (STSTB) is achieved.



EXAMPLE: (8080 t_{CY} = 500ns)
OSC = 18mHz/55ns
 ϕ_1 = 110ns (2 x 55ns)
 ϕ_2 = 275ns (5 x 55ns)
 $\phi_2 - \phi_1$ = 110ns (2 x 55ns)

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STSTB (Status Strobe)

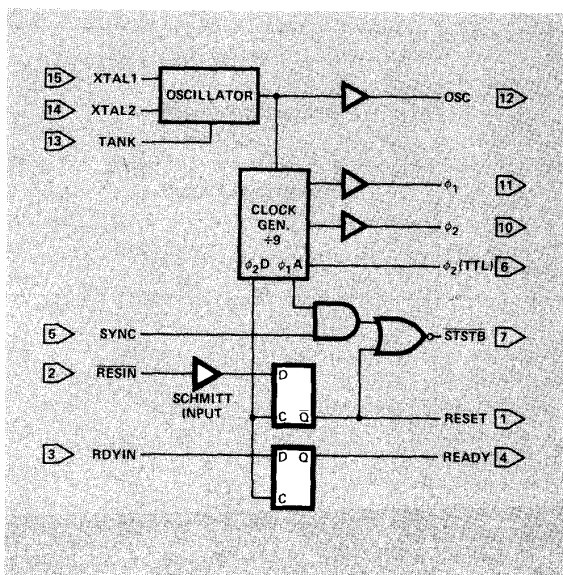
At the beginning of each machine cycle the 8080A CPU issues status information on its data bus. This information tells what type of action will take place during that machine cycle. By bringing in the SYNC signal from the CPU, and gating it with an internal timing signal (ϕ_1A), an active low strobe can be derived that occurs at the start of each machine cycle at the earliest possible moment that status data is stable on the bus. The \overline{STSTB} signal connects directly to the 8228 System Controller.

The power-on Reset also generates \overline{STSTB} , but of course, for a longer period of time. This feature allows the 8228 to be automatically reset without additional pins devoted for this function.

Power-On Reset and Ready Flip-Flops

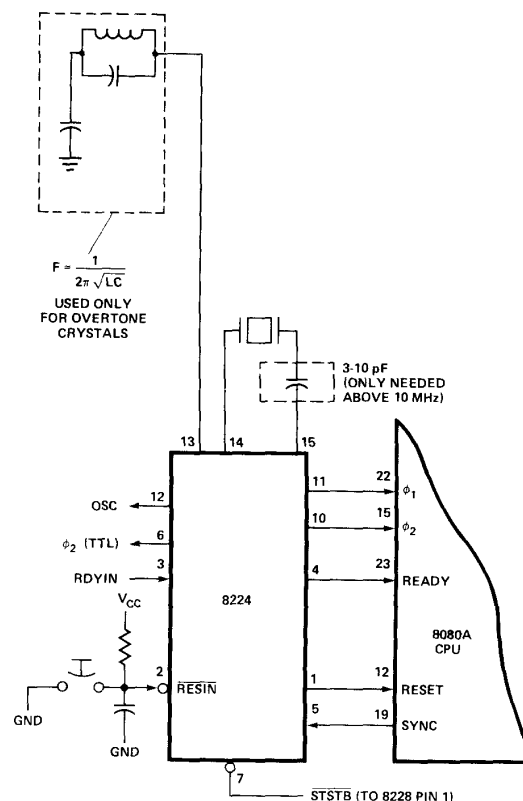
A common function in 8080A Microcomputer systems is the generation of an automatic system reset and start-up upon initial power-on. The 8224 has a built in feature to accomplish this feature.

An external RC network is connected to the \overline{RESIN} input. The slow transition of the power supply rise is sensed by an internal Schmitt Trigger. This circuit converts the slow transition into a clean, fast edge when its input level reaches a predetermined value. The output of the Schmitt Trigger is connected to a "D" type flip-flop that is clocked with ϕ_2D (an internal timing signal). The flip-flop is synchronously reset and an active high level that complies with the 8080A input spec is generated. For manual switch type system Reset circuits, an active low switch closing can be connected to the \overline{RESIN} input in addition to the power-on RC network.



The READY input to the 8080A CPU has certain timing specifications such as "set-up and hold" thus, an external synchronizing flip-flop is required. The 8224 has this feature built-in. The RDYIN input presents the asynchronous "wait request" to the "D" type flip-flop. By clocking the flip-flop with ϕ_2D , a synchronized READY signal at the correct input level, can be connected directly to the 8080A.

The reason for requiring an external flip-flop to synchronize the "wait request" rather than internally in the 8080 CPU is that due to the relatively long delays of MOS logic such an implementation would "rob" the designer of about 200ns during the time his logic is determining if a "wait" is necessary. An external bipolar circuit built into the clock generator eliminates most of this delay and has no effect on component count.



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D.C. Characteristics

$T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = +5.0\text{V} \pm 5\%$; $V_{DD} = +12\text{V} \pm 5\%$.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Current Loading			-.25	mA	$V_F = .45\text{V}$
I_R	Input Leakage Current			10	μA	$V_R = 5.25\text{V}$
V_C	Input Forward Clamp Voltage			1.0	V	$I_C = -5\text{mA}$
V_{IL}	Input "Low" Voltage			.8	V	$V_{CC} = 5.0\text{V}$
V_{IH}	Input "High" Voltage	2.6 2.0			V	Reset Input All Other Inputs
$V_{IH}-V_{IL}$	REDIN Input Hysteresis	.25			mV	$V_{CC} = 5.0\text{V}$
V_{OL}	Output "Low" Voltage			.45	V	(ϕ_1, ϕ_2) , Ready, Reset, $\overline{\text{STSTB}}$ $I_{OL} = 2.5\text{mA}$ All Other Outputs $I_{OL} = 15\text{mA}$
				.45	V	
V_{OH}	Output "High" Voltage	9.4 3.6 2.4			V	$I_{OH} = -100\mu\text{A}$ $I_{OH} = -100\mu\text{A}$ $I_{OH} = -1\text{mA}$
	ϕ_1, ϕ_2				V	
	READY, RESET All Other Outputs				V	
$I_{SC}^{(1)}$	Output Short Circuit Current (All Low Voltage Outputs Only)	-10		-60	mA	$V_O = 0\text{V}$ $V_{CC} = 5.0\text{V}$
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

CRYSTAL REQUIREMENTS

Tolerance: .005% at 0°C - 70°C

Resonance: Series (Fundamental) *

Load Capacitance: 20-35pF

Equivalent Resistance: 75-20 ohms

Power Dissipation (Min): 4mW

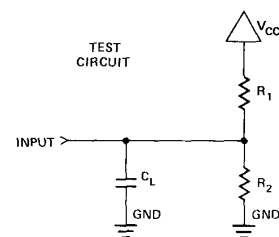
*With tank circuit use 3rd overtone mode.

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A.C. Characteristics

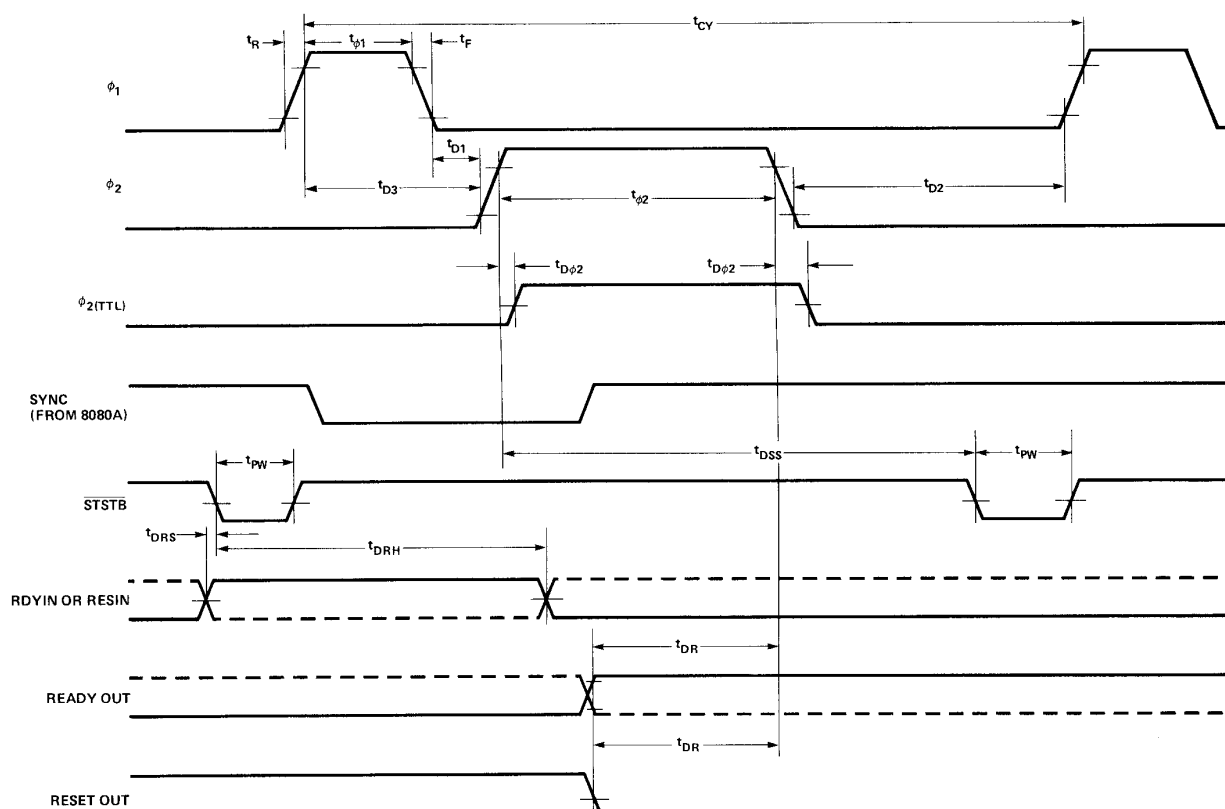
$V_{CC} = +5.0V \pm 5\%$; $V_{DD} = +12.0V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9} - 20ns$			ns	$C_L = 20pF$ to $50pF$
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9} - 35ns$				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9} - 14ns$				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9} + 20ns$		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	ϕ_2 TTL, $C_L=30$ $R_1=300\Omega$ $R_2=600\Omega$
t_{DSS}	ϕ_2 to \overline{STSTB} Delay	$\frac{6tcy}{9} - 30ns$		$\frac{6tcy}{9}$		\overline{STSTB} , $C_L=15pF$ $R_1 = 2K$ $R_2 = 4K$
t_{PW}	\overline{STSTB} Pulse Width	$\frac{tcy}{9} - 15ns$				
t_{DRS}	RDYIN Setup Time to Status Strobe	$50ns - \frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After \overline{STSTB}	$\frac{4tcy}{9}$				
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	$\frac{4tcy}{9} - 25ns$				Ready & Reset $C_L=10pF$ $R_1=2K$ $R_2=4K$
t_{CLK}	CLK Period		$\frac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency	27			MHz	
C_{in}	Input Capacitance			8	pF	$V_{CC}=+5.0V$ $V_{DD}=+12V$ $V_{BIAS}=2.5V$ $f=1MHz$



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WAVEFORMS



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

EXAMPLE:

A.C. Characteristics (For $t_{CY} = 488.28$ ns)

$T_A = 0^\circ\text{C}$ to 70°C ; $V_{DD} = +5\text{V} \pm 5\%$; $V_{DD} = +12\text{V} \pm 5\%$.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	$t_{CY}=488.28\text{ns}$ ϕ_1 & ϕ_2 Loaded to $C_L = 20$ to 50pF
$t_{\phi 2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to \overline{STSTB} Delay	296		326	ns	Ready & Reset Loaded to $2\text{mA}/10\text{pF}$ All measurements referenced to 1.5V unless specified otherwise.
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	
t_{DRS}	RDYIN Setup Time to \overline{STSTB}	-167			ns	
t_{DRH}	RDYIN Hold Time after \overline{STSTB}	217			ns	
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	
f_{MAX}	Oscillator Frequency			18.432	MHz	